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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,065	06/16/2004	Brian T. Denton	BUR920040051US1	4064

45093 7590 03/31/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2121	

NOTIFICATION DATE	DELIVERY MODE
03/31/2010	ELECTRONIC

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BRIAN T. DENTON,
CUC K. HUYNH, SHREESH S. TANDEL,
and STEVEN H. VOLDMAN

Appeal 2009-002960
Application 10/710,065[1]
Technology Center 2100

Decided: March 29, 2010

Before JOHN A. JEFFERY, LEE E. BARRETT, and JAY P. LUCAS, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-35. We have jurisdiction pursuant to 35 U.S.C. § 6(b).

We affirm-in-part.

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[1] Filed June 16, 2004, titled "Optimized Scheduling Based on Sensitivity Data." The real party in interest is International Business Machines Corporation.

STATEMENT OF THE CASE

The invention

The invention relates to a scheduling optimizer system, method and program product that analyzes a device for sensitivities, such as electrostatic discharge (ESD) sensitivities, and allows for modification of a floor schedule of the assembly unit of the device based on the sensitivity of the device.

Illustrative claim

Claim 1 is reproduced below for illustration:

1. A method comprising the steps of:

a. providing a floor schedule of an assembly unit for a device;

b. optimizing the floor schedule based on sensitivity data of the device during operation of the assembly unit on the floor schedule; and

operating the assembly unit based on the optimized floor schedule.

The references

Shirley	US 6,351,684 B1	Feb. 26, 2002
Miller	US 6,535,783 B1	Mar. 18, 2003
Conboy	US 6,711,450 B1	Mar. 23, 2004
Kraz	US 2004/0082083 A1	Apr. 29, 2004
Chong	US 6,842,661 B2	Jan. 11, 2005 (filed Sep. 30, 2002)

The rejections

Claims 12-18 stand rejected under 35 U.S.C. § 101 as directed to nonstatutory subject matter.

Claims 1, 2, 4, 7-10, 12-16, 18-21, 23, 24, 26, 27, and 29-31 stand rejected under 35 U.S.C. § 102(e) as anticipated by Chong.

Claims 3 and 28 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Chong and Kraz.

Claims 11, 22, and 32-35 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Chong and Miller.

Claims 5 and 17 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Chong and Conboy.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Chong and Conboy, further in view of Shirley.

Claim 25 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Chong and Miller, further in view of Conboy.

PATENTABLE SUBJECT MATTER

The Examiner finds that "computer usable medium" has not been defined in the Specification and given its broadest reasonable interpretation, is consistent with transitory waves and carrier waves, which are not patentable subject matter. Final Office Action (FOA) 3.

Appellants do not mention or argue the § 101 rejection. Accordingly, the rejection of claims 12-18 under 35 U.S.C. § 101 is affirmed *pro forma*. *See* MPEP § 1205.02 ("If a ground of rejection stated by the examiner is not

addressed in the appellant's brief, that ground of rejection will be summarily sustained by the Board.").

ANTICIPATION

Issue

Does Chong teach "optimizing the floor schedule based on sensitivity data of the device," as recited in independent claim 1? In particular, does Chong teach "sensitivity data"?

Independent claim 12 recites "program code configured to optimize the floor schedule of the assembly unit based on the sensitivity data." Independent claim 19 recites "a scheduling optimizer for optimizing the floor schedule of the assembly unit based on the analyzed sensitivity data." Independent claim 26 recites "receiving an optimal path data of the floor schedule that is generated based on the sensitivity data." Thus, the claims rejected under § 102 all recite "sensitivity data" and the claims will be treated as standing or falling together with claim 1.

Principles of law

Claim interpretation

The words of a claim are generally given their "ordinary and customary meaning" where "the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). After the claims, the patent's specification is "the

single best guide to the meaning of a disputed term." *Id.* at 1315. "[T]he specification 'acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication.'" *Id.* at 1321.

Anticipation

"Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim." *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983).

In addition, the prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public. *Akzo N.V. v. U.S. Intern. Trade Com'n*, 808 F.2d 1471, 1479 (Fed. Cir. 1986).

Findings of fact

Specification

The Specification refers numerous times to "sensitivity," but does not expressly define the term.

The Specification describes that data may include "sensitivity data of the device (e.g., ESD sensitivity data, or similar data involving risk factors of the device)." ¶ 0033.

The Specification describes, in the context of sensitivity to electrostatic discharge (ESD), how sensitivity data is generated:

> One example of generating sensitivity data is through generating statistical "sensitivity models." Sensitivity models represent the ESD failures of a device and may be used to estimate the yield factors of an assembly lot to determine if the floor schedule of the assembly lot or device should be optimized. Some examples of sensitivity models

> that are well-known in the art include: human body models (HBM); machine models (MM); charges device models (CDM); transmission line pulse (TLP), very fast transmission line pulse (VF-TLP), and cable discharge models; and cassette models, etc. Sensitivity models such as HBM, MM and CDM may be obtained through a simple resistor/capacitor circuit and are represented by the magnitude of the resulting waveform.

¶ 0044.

Chong

Chong relates to semiconductor manufacturing, and more particularly, to a method and apparatus for performing process control at an interconnect level on a workpiece. Col. 1, ll. 8-11.

Chong describes that in the prior art, characterization of interconnect parameters was made when processing was substantially complete, so there was an inherent lack of feedback correction ability. Col. 2, ll. 35-52.

Chong describes acquiring manufacturing data relating to an interconnect location on the workpiece and an interconnect characteristic control process is performed based upon the manufacturing data. Col. 2, ll. 60-63. The interconnect characteristic data can be based on "wafer electrical test (WET)" data and "metrology" data. Figure 10. "Upon analysis of the metrology data and/or the WET data, the system 300 may implement an interconnect characteristic control process to affect the characteristics of interconnect locations (e.g., vias, contact, etc.) on the semiconductor wafers 105 (block 1060)." Col. 9, ll. 27-31.

Chong describes "a wafer electrical test (WET) unit 330 that is capable of performing a plurality of electrical tests that provide data relating to the electrical characteristics of various interconnect locations (e.g., contacts and/or vias) on the semiconductor wafers 105" (col. 5, lines 10-14) and "[t]he system 300 is capable of performing various control adjustments to affect the characteristics of various interconnect locations on the semiconductor wafers 105, e.g., controlling the resistivity of a via and/or a contact" (col. 5, ll. 32-35). The electrical characteristic of the interconnect locations described (col. 5, l. 65 to col. 7, l. 17) is "resistivity."

Chong further describes metrology as follows:

> The metrology data analysis unit 960 may collect, organize, and analyze data from the metrology tool 950. The metrology data is directed to a variety of physical or electrical characteristics of the devices formed across the semiconductor wafers 105. For example, metrology data may be obtained as to line width measurements, depth of trenches, sidewall angles, thickness, resistance, and the like.

Col. 8, ll. 48-55. That is, metrology data may be physical or electrical data.

Claim interpretation

Proper claim interpretation necessarily precedes a determination of patentability. *See Gechter v. Davidson*, 116 F.3d 1454, 1457 (Fed. Cir. 1997) ("Implicit in our review of the Board's anticipation analysis is that the claim must first have been correctly construed to define the scope and meaning of each contested limitation."). The issue here is the meaning of "sensitivity data."

Appellants state that sensitivity is defined as a degree of change in one thing in response to a unit amount of change in another thing. Br. 5. The Examiner seems to accept Appellants' definition of sensitivity because it is stated: "In summary, per Appellant's definition above, Chong discloses sensitivity data as to a change of electrical characteristics (e.g. resitivity [sic]) in response to a change metrology data (i.e. physical or electrical characteristics) and/or control data." Ans. 24.

The Specification describes "sensitivity models" in the context of sensitivity to electrostatic discharge (ESD) where "[s]ensitivity models such as HBM, MM and CDM may be obtained through a simple resistor/capacitor circuit and are represented by the magnitude of the resulting waveform." ¶ 0044. This provides guidance as to measurement of sensitivity data. One of ordinary skill in the art, if he or she did not already know what was meant by "sensitivity data," would have reasonably looked to various articles and other technical references describing such models. One such article is "Device Sensitivity and Testing," http://www.ce-mag.com/99ARG/ESD%20Assoc185.html (last visited Mar. 11, 2010), which discusses the three primary models of ESD events: HBM, MM, and CDM. This article is consistent with Appellants' definition.

The Specification describes that data may include "sensitivity data of the device (e.g. ESD sensitivity data, or similar data involving risk factors of the device)." ¶ 0033. This indicates that sensitivity data may include data involving risk factors of the device.

Therefore, "sensitivity" is defined as "a degree of change in one thing in response to a unit amount of change in another thing" where the "change" can mean failure in response to an ESD event of a certain magnitude, i.e., sensitivity does not require a continuous change in a variable.

Analysis

The Examiner finds that data relating to "physical or electrical characteristics" includes "sensitivity data." The Examiner refers to column 5, lines 10-35; column 5, line 65 to column 6, line 35; column 7, lines 18-35; column 8, lines 48-52; and column 9, lines 27-33.

Appellants argue the "electrical characteristics" or "metrology data" in Chong do not include sensitivity data and thus, Chong does not disclose optimizing a floor schedule based on sensitivity data. Br. 5. It is argued that the "electrical characteristics" are not equivalent to "data involving risk factors of the device" because a risk factor is a change in a variable in response to a change in another variable. Br. 5-6. It is argued that Chong "does not enable an implementation of 'optimizing the floor schedule based on sensitivity data of the device' (claim 1) because the disclosed resistivity detecting and controlling does not enable a person of skill to instead implement optimizing a floor plan based on sensitivity data of the device without undue experimentation." Br. 6.

Chong describes "a wafer electrical test (WET) unit 330 that is capable of performing a plurality of electrical tests that provide data relating to the electrical characteristics of various interconnect locations (e.g.,

contacts and/or vias) on the semiconductor wafers 105." Col. 5, lines 10-14. Chong also describes "metrology data is directed to a variety of physical or electrical characteristics of the devices formed across the semiconductor wafers 105. For example, metrology data may be obtained as to line width measurements, depth of trenches, sidewall angles, thickness, resistance, and the like." Col. 8, ll. 50-55. Based on these teachings, the Examiner's position is: "In summary, per Appellant's definition above, Chong discloses sensitivity data as to a change of electrical characteristics (e.g. resitivity [sic]) in response to a change metrology data (i.e. physical or electrical characteristics) and/or control data." Ans. 24.

The Examiner's statement, however, does not clearly explain how the electrical characteristics measured by the WET unit (resistivity) and the electrical and physical characteristics measured by the metrology tool (line width measurements, depth of trenches, sidewall angles, thickness, resistance, and the like) fall within the definition of "sensitivity data." Manifestly, just measuring an individual physical or electrical characteristic does not measure sensitivity. We interpret the Examiner's statement that resistivity is changed in response to a change in metrology data to mean that when electrical or physical characteristics are changed, the resistivity is affected. While it is true that changes in the physical and electrical characteristics of the chip affect the resistivity, e.g., the composition of the barrier layer and the film thickness of the layers that form the barrier layer affect resistivity (col. 6, ll. 26-32), sensitivity data requires more than a change in one factor affecting another factor: there must be a relationship

expressing that one factor is affected by the other. For example, the operability of semiconductor chips is "sensitive to" ESD of a certain voltage, as taught in Kraz, some electronics are "sensitive to" vibration above a certain amount, etc. There is no teaching or suggestion that the relationship between any physical change and any resulting electrical change is in anyway tracked or noted in Chong so that one is "sensitive" to another. Accordingly, Chong does not teach "sensitivity data."

Conclusion

Chong does not teach "optimizing the floor schedule based on sensitivity data of the device," as recited in independent claim 1 and similar limitations in independent claims 12, 19, and 26. The anticipation rejection of claims 1, 2, 4, 7-10, 12-16, 18-21, 23, 24, 26, 27, and 29-31 is reversed.

OBVIOUSNESS

Claims 32-35

Independent claim 32 recites "a sensitivity monitor for generating sensitivity data for a device; a reliability generator for generating reliability data having rules for the device; and a tool controller for invoking the sensitivity monitor and reliability generator and shutting down a testing tool of the testing unit." The Examiner cites Miller for the limitation of "shutting down a testing tool of the testing unit." Ans. 16. Appellants argue that Chong does not disclose "generating sensitivity data for a device" and Miller

does not cure the deficiency of Chong. Br. 7. The Examiner maintains that the limitation is taught by Chong and does not rely on Miller. Ans. 26.

Because Chong does not teach "sensitivity data," and the Examiner does not rely on Miller for this limitation, the rejection of claims 32-35 is reversed.

Claims 11 and 22

Because Chong does not teach "sensitivity data," as recited in independent claims 1 and 19, and the Examiner does not rely on Miller for this limitation (Ans. 35), the rejection of claims 11 and 22 is reversed.

Claims 3 and 28

Contentions

Claims 3 and 28 recite that "the sensitivity data includes at least one of electrostatic discharge sensitivity data, electrical overstress sensitivity data, latch-up data, hot electron data, mobile ion contamination data, and negative bias threshold instability data." The Examiner finds that Chong does not teach this limitation, but finds that "Kraz teaches [] measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool" (FOA 11) and concludes that it would have been obvious to modify Chong to provide for measuring and monitoring electrostatic discharge and electrostatic voltage "to provide the automatic detection and response to an ESD event" (FOA 11).

Appellants argue:

> Kraz monitors the ESD occurrences inside a semiconductor manufacturing tool (*see* paragraph 0034) regarding the source, strength and frequency of the ESDs (*see* paragraph 0025), but does not monitor electrostatic discharge sensitivity data of the processed devices. In addition, the claimed invention includes ESD sensitivity data of the device manufactured, not the ESD occurrence inside the process tool as disclosed in Kraz.
>
> The Examiner argued that Kraz discloses that the monitored ESD occurrences can be used for failure analysis (Office Action at page 11, citing Kraz at paragraph 0028), however, the peripheral mentioning of failure analysis is not equivalent to optimizing the floor schedule based on, e.g., the ESD sensitivity data, because Kraz does not disclose obtaining ESD sensitivity data.

Br. 7-8.

Issue

We find that Chong does not teach "sensitivity data." Therefore, assuming Kraz teaches measuring sensitivity data, it is difficult to say why one skilled in the art would have modified Chong. Nevertheless, Kraz mentions "ESD sensitivity" (¶ 0002) and Figure 1 of Kraz shows a graph of ESD sensitivities for different technologies, so we must consider whether Kraz itself may be a better reference than Chong.

The issue is:

Does Kraz cure the deficiencies of Chong with respect to the limitation of "optimizing the floor schedule based on sensitivity data of the device," in independent claim 1 and the similar limitations in claim 26?

Principles of law

"[T]he test [for obviousness] is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). A rejection under 35 U.S.C. § 103(a) is based on the following factual determinations: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 399 (2007) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). "[H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418. "A person of ordinary skill is also a person of ordinary creativity, not an automaton." *Id.* at 421.

If the rejection of a dependent claim is affirmed, the rejection of the independent claim from which it depends is also affirmed. *See Aventis Pharma Deutschland GmbH v. Lupin, Ltd.*, 499 F.3d 1293, 1300 (Fed. Cir. 2007); *Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1319-20 (Fed. Cir. 2007) (law of the case that a dependent claim was obvious means the parent claim must also have been obvious); *In re Muchmore*, 433 F.2d 824, 825 (CCPA 1970) ("Since we agree with the board's conclusion of obviousness as to these narrow claims, the broader claims must likewise be obvious.").

Findings of fact

Kraz describes monitoring an ESD occurrence in a semiconductor process tool. ¶¶ 0009, 0031-32. This may be done "to determine the source, strength and frequency of those ESD occurrences (including electrostatic discharge or electrostatic voltage) in order to increase the yield of the semiconductor process." ¶ 0025.

Kraz teaches that the process of sorting out integrated circuits (ICs) that were exposed to dangerous levels of ESD can be automated and requires no operator assistance. ¶¶ 0011; 0106.

Kraz describes:

> When a test program is entered for each IC, ESD thresholds (damage and latent damage) are also entered as parameters. The software of the handler then sets threshold of Event monitor for each point in accordance with IC damage level and antenna distance from the IC in process. It is recommended that the level determined to cause latent damage be entered as the threshold. This way, all ESD occurrences (including electrostatic discharge or electrostatic voltage) below this level will be discarded by the Event monitor. As an example, the damage level of an IC is set to 200V CDM model and the latent damage threshold is set to 150V CDM. "Chip down" signals for each particular operation are communicated by the handler to Event monitoring system during operation of the handler. Event monitoring system provides IC handler with flow of data corresponding to magnitude of ESD occurrences (including electrostatic discharge or electrostatic voltage) at each particular location.
>
> In step 52, the system determines that an ESD occurrence event has occurred. In step 54, the system determines if the captured ESD occurrence is above the damage threshold. If an IC is exposed to ESD occurrence of stronger magnitude than the damage threshold, then IC handler would automatically place this IC into a separate tray in step

> 56. In step 58, the system determines if the ESD occurrence is above the latent threshold near the appropriate sensor near the IC in step 60. If the IC experienced a lesser discharge, but still higher than the latent damage threshold, it can be automatically placed in a re-test tray in step 62 for future re-test and analysis by reliability engineer in step 64. Using this integrated process, the customer is assured that no IC that was exposed to excessive ESD levels is shipped to a customer.

¶¶ 0106-0107.

Analysis

The levels determined to cause latent damage to the IC are considered to be "sensitivity data." Thus, "the damage level of an IC is set to 200V CDM model and the latent damage threshold is set to 150V CDM" (¶ 0106) are "electrostatic discharge sensitivity data" as recited in claim 3 for the particular IC. Kraz teaches more than just measuring ESD.

The other limitations of claim 1 are very broad and appear to be met by Kraz. Thus, "providing a floor schedule of an assembly unit for a device" broadly includes a schedule of passing the device being assembled from one tool to the next. The limitation of "optimizing the floor schedule based on sensitivity data of the device during operation of the assembly unit on the floor schedule" is broad enough to read on revising the schedule to move the IC to a different tray based on the ESD sensitivity data, i.e., if an ESD event exceeds an ESD sensitivity threshold, the schedule is changed. The last step of "operating the assembly unit based on the optimized floor schedule" only requires actually carrying out the planned IC move. For this reason, Kraz alone teaches or makes obvious the subject matter of claims 1 and 3. This is

a case where the added reference "cures the deficiency" in the rejection of the parent claim. The rejection of claim 3 is affirmed. Parent claim 1, although not explicitly rejected under § 103(a), is considered implicitly rejected as unpatentable since if a dependent claim is obvious this means the parent claim must also have been obvious. *See Aventis*, 499 F.3d at 1300; *Ormco*, 498 F.3d at 1319-20; *Muchmore*, 433 F.2d at 825. Thus, we affirm the obviousness rejection of claim 3 and parent claim 1. We do not examine the other claims dependent upon claim 1.

Claim 26 presents a different issue. Claim 26 recites "generating sensitivity data for a device of an assembly unit during operation of the assembly unit on a floor schedule," which requires generating sensitivity data during operation. Claim 1 required optimizing the floor schedule during operation. Kraz does not appear to teach, that we can find, generating the sensitivity data during operation, but feeds this information in at the beginning of the process. Accordingly, we conclude that neither Kraz nor the combination of Chong and Kraz make obvious the subject matter of claims 26 and 28. The rejection of claim 28 is therefore reversed.

Claims 5 and 17

Because Chong does not teach "sensitivity data," as recited in independent claims 1 and 12, and the Examiner does not rely on Conboy for this limitation (Ans. 36), the rejection of claims 5 and 17 is reversed.

Claim 6

Because Chong does not teach "sensitivity data," as recited in independent claim 1, and the Examiner does not rely on Conboy or Shirley for this limitation (Ans. 36), the rejection of claim 6 is reversed.

Claim 25

Because Chong does not teach "sensitivity data," as recited in independent claim 19, and the Examiner does not rely on Miller or Conboy for this limitation (Ans. 37), the rejection of claim 25 is reversed.

CONCLUSION

The rejection of claims 12-18 under 35 U.S.C. § 101 is affirmed.

The rejection of claims 1, 2, 4, 7-10, 12-16, 18-21, 23, 24, 26, 27, and 29-31 under 35 U.S.C. § 102(e) is reversed.

The rejection of claim 3 under 35 U.S.C. § 103(a) is affirmed. The rejection implicitly includes a rejection of claim 1 because claim 3 includes all the limitations of claim 1. Thus, the rejection of claim 1 is affirmed for the reasons stated with respect to claim 3.

The rejections of claims 5, 6, 11, 17, 22, 25, 28, and 32-35 under 35 U.S.C. § 103(a) are reversed.

Requests for extensions of time are governed by 37 C.F.R. § 1.136(b).

See 37 C.F.R. § 41.50(f).

AFFIRMED-IN-PART

Attachment:

The ESD Ass'n, *Device Sensitivity and Testing*, Compliance Eng'g, http://www.cemag.com/99ARG/ESD%20Assoc185.html (last visited Mar. 11, 2010)

rwk

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Feature Article

Device Sensitivity and Testing

By The ESD Association

Device failure models and test methods define the sensitivity of electronic devices and assemblies that need to be protected from the effects of ESD. This key information can help you design a more effective ESD control program.

Two of the key elements in any successful static-control program are the identification of those items—whether components, assemblies, or finished products—that are sensitive to ESD, and the determination of the level of their sensitivity. The damage done to an electrostatic-discharge-sensitive (ESDS) device by an ESD event will depend on the device's ability either to dissipate the energy of the discharge or to withstand the current levels involved. This is known as device ESD sensitivity or ESD susceptibility.

Certain devices may be more readily damaged by discharges occurring within automated equipment, while others may be more prone to damage from handling by personnel. In this article, we will review the models and test procedures used to characterize, determine, and classify the sensitivity of components to ESD. These test procedures are based on the three primary models of ESD events: human body model (HBM), machine model (MM), and charged device model (CDM). While the models employed to perform component testing cannot replicate the full spectrum of all possible ESD events, they have proven to be successful in reproducing over 95% of all ESD field-failure signatures. The use of standardized test procedures has allowed the industry to:

- Develop and measure suitable on-chip protection.
- Make comparisons among various devices.
- Provide a system of ESD-sensitivity classification to assist in the ESD design and ESD monitoring requirements of the manufacturing and assembly environments.
- Ensure reliable and repeatable test results.

Human Body Model

One of the common causes of electrostatic damage is the direct transfer of electrostatic charge through a significant series resistor (±1.5k ohms) from either the human body or a charged material to the ESDS device. When a person walks across a floor, an electrostatic charge accumulates on his or her body. Simple contact of a finger to the leads of an ESDS device or assembly permits the body to discharge, possibly causing device damage. The model used to simulate this event is called the Human Body Model, or HBM.

HBM is the oldest and most commonly used method of classifying device sensitivity to ESD. The testing model, which represents the discharge delivered to the device from the fingertip of a standing individual, comprises a 100-pF capacitor discharged through a switching component and a 1.5k-ohm series resistor into the component. Dating from the nineteenth century, this model was originally developed for the purpose of investigating explosive gas mixtures in mines. It was adopted by the military in MIL-STD-883 Method 3015 and is also used in ESD Association standard ESD-STM5.1-1998—Device Testing: Human Body Model. The HBM circuit is illustrated in Figure 1.

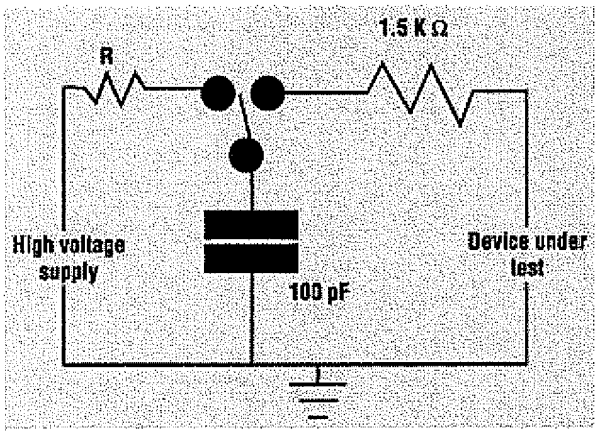

Figure 1. Typical human body model (HBM) circuit.

Testing for HBM sensitivity is generally performed using automated test systems, with the devices being placed in the test system and contacted through a relay matrix. After ESD zaps are applied, the post-stress I-V current traces are reviewed to see if the device has failed. The ESD Association's HBM test standard has been revised and includes several new technical changes. First, the number of zaps per stress level and polarity has been reduced, from three to one. The minimum time interval between zaps has also been reduced, from one second to 300 milliseconds. Taken together, these modifications serve to cut the total HBM qualification test time.

The second major technical change is a revision in the HBM tester specifications: the maximum rise time for an HBM waveform measured through a 500-ohm load has been increased from 20 to 25 nanoseconds. This will allow manufacturers of HBM test equipment to build high-pin-count testers, which typically have a higher parasitic test-board capacitance that slows down the 500-ohm

waveform.

Machine Model

Another kind of discharge, similar to the HBM event, can occur from a charged conductive object such as a metallic tool or fixture. Originating in Japan as a result of attempts to create a worst-case HBM event, this ESD model, known as the machine model (MM), consists of a 200-pF capacitor discharged directly into a component, with no series resistor (see Figure 2).

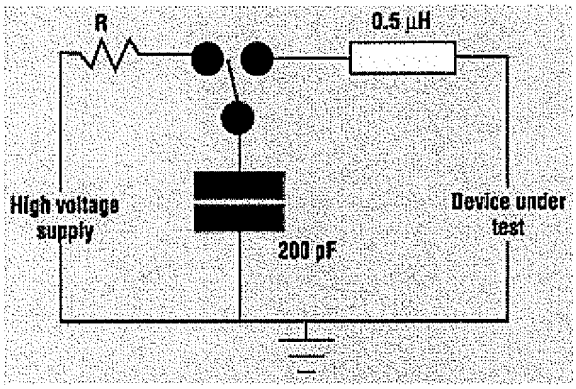

Figure 2. Typical machine model (MM) circuit.

As a worst-case HBM, the machine model may be overly severe. However, there are certain real-world situations that this model represents—for example, the rapid discharge from a charged board assembly or from the charged cables of an automatic tester.

The testing of devices for MM sensitivity using ESD Association standard *ANSI/ESD-S5.2-1994—Device Testing: Machine Model* is much like HBM testing. But while the test equipment used for the two models is the same, the test head is slightly different, in that the MM version does not have a 1.5k ohm resistor. (The test board and the socket replicate those employed for HBM testing.)

Charged Device Model

The transfer of charge from an ESDS device is also an ESD event. A device may, for instance, become charged when sliding down the feeder in an automated assembler. If it then contacts the insertion head or some other conductive surface, a rapid discharge may occur from the device to the metal object. This so-called charged device model (CDM) event can be even more destructive than the HBM event for some devices. Although the duration of the discharge is very short—often less than one nanosecond—the peak current can reach several tens of amperes.

Several test methods have been explored to duplicate the real-world CDM event and replicate the conditions that have been observed in CDM-caused field failures. Efforts in this area are currently focusing on two separate test methods. The first, known as CDM, better simulates an actual charged-device event, while the second

addresses devices that are inserted into a socket and then charged and discharged in the same socket. This second method is termed the socketed discharge model, or SDM.

A draft standard for CDM, designated ESD-DS5.3.1-1996—Device Testing: Charged Device Model, was released in 1996. (Work is ongoing to release a full standard in the near future.) The test procedure involves placing the device on a field plate with its leads pointing up, then charging and discharging it. Figure 3 illustrates a typical CDM test setup.

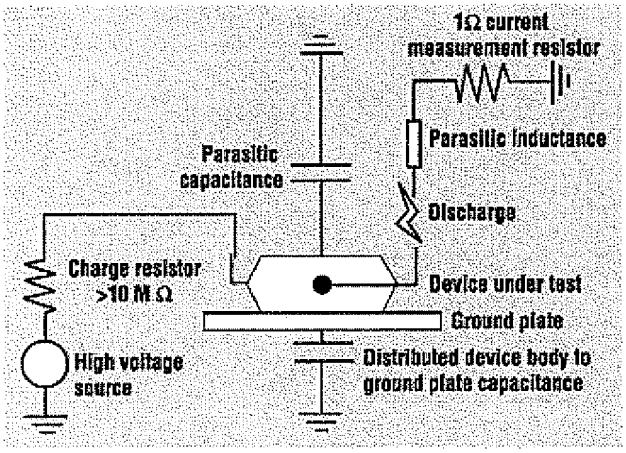

Figure 3. Typical charged device model (CDM) test circuit.

SDM testing is similar to testing for HBM and MM sensitivity. The device is placed in a socket, charged from a high-voltage source, and then discharged. This procedure remains a work in progress and still has a number of limitations, including too great a dependence on the specific design of the SDM tester.

Device Sensitivity Classification

Each of the device-testing methods provides a classification system for defining the component's sensitivity to the specified model (see Tables I, II, and III). These classification systems have a couple of advantages: first, they allow for easy grouping and comparison of components according to their ESD sensitivity; second, they give an indication of the level of ESD protection required for a particular component.

Class	Voltage (V) range
Class 0	<250 V
Class 1A	250 to < 500 V
Class 1B	500 to < 1000 V
Class 1C	1000 to < 2000 V
Class 2	2000 to < 4000 V
Class 3A	4000 to < 8000 V

Class 3B	> 8000 V

Table I. ESDS component sensitivity classification, human body model (per ESD STM5.1-1998).

Class	Voltage (V) range
Class M0	<25 V
Class M1	25 to < 100 V
Class M2	100 to < 200 V
Class M3	200 to < 400 V
Class M4	400 to < 800 V
Class M5	> 800 V

Table II. ESDS component sensitivity classification, machine model (per ANSI/ESD-S5.2-1994).

Class	Voltage (V) range
Class C0	<125 V
Class C1	125 to < 250 V
Class C2	250 to < 500 V
Class C3	500 to < 1000 V
Class C4	1000 to < 2000 V
Class C5	> 2000 V

Table III. ESDS component sensitivity classification, charged device model (per EOS/ESD-DS5.3.1-1996).

A fully characterized component should be classified using all three models—the HBM, the MM, and the CDM. For example, a fully characterized component may have the following designations: Class 1B (500 to < 1000 V HBM), Class M1 (25 to < 100 V MM), and Class C3 (500 to < 1000 V CDM). This would alert a potential user of the component to the need for a controlled environment, whether assembly and manufacturing operations are performed by human beings or by machines.

A word of caution is in order, however. These classification systems and component-sensitivity test results should function as guides, not necessarily as absolutes. The events defined by the test procedures produce narrowly restrictive data that must be carefully considered and judiciously used. The three ESD models represent discrete points developed in an attempt to characterize ESD vulnerability. The data points are informative and useful, but their arbitrary extrapolation into a real-world scenario can be misleading. The true value of the data lies in comparing one device with another and in providing a starting place for the establishment of an effective ESD-control program.

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